

The timing diagram illustrates the relationship between the 68000 microprocessor and its external devices. The signals shown are:

- CLK**: Clock signal, a continuous square wave.
- AD**: Address/Data bus, which carries the address during the first two clock cycles of each instruction and the data during the subsequent cycles.
- FRAME**: Frame signal, which is active (low) during the first two clock cycles of each instruction.
- IRDY**: Input Ready signal, which is active (low) when the processor is ready to receive data.
- TRDY**: Output Ready signal, which is active (low) when the processor is ready to send data.
- DEVSEL**: Device Select signal, which is active (low) when the processor is selecting a device.

The diagram is divided into three sections labeled 0, 1, and 2, each showing 10 clock cycles. The signals are synchronized with the clock, and the FRAME signal is active during the first two clock cycles of each instruction. The IRDY and TRDY signals are active during the first two clock cycles of each instruction, and the DEVSEL signal is active during the first two clock cycles of each instruction.

FIG. 3

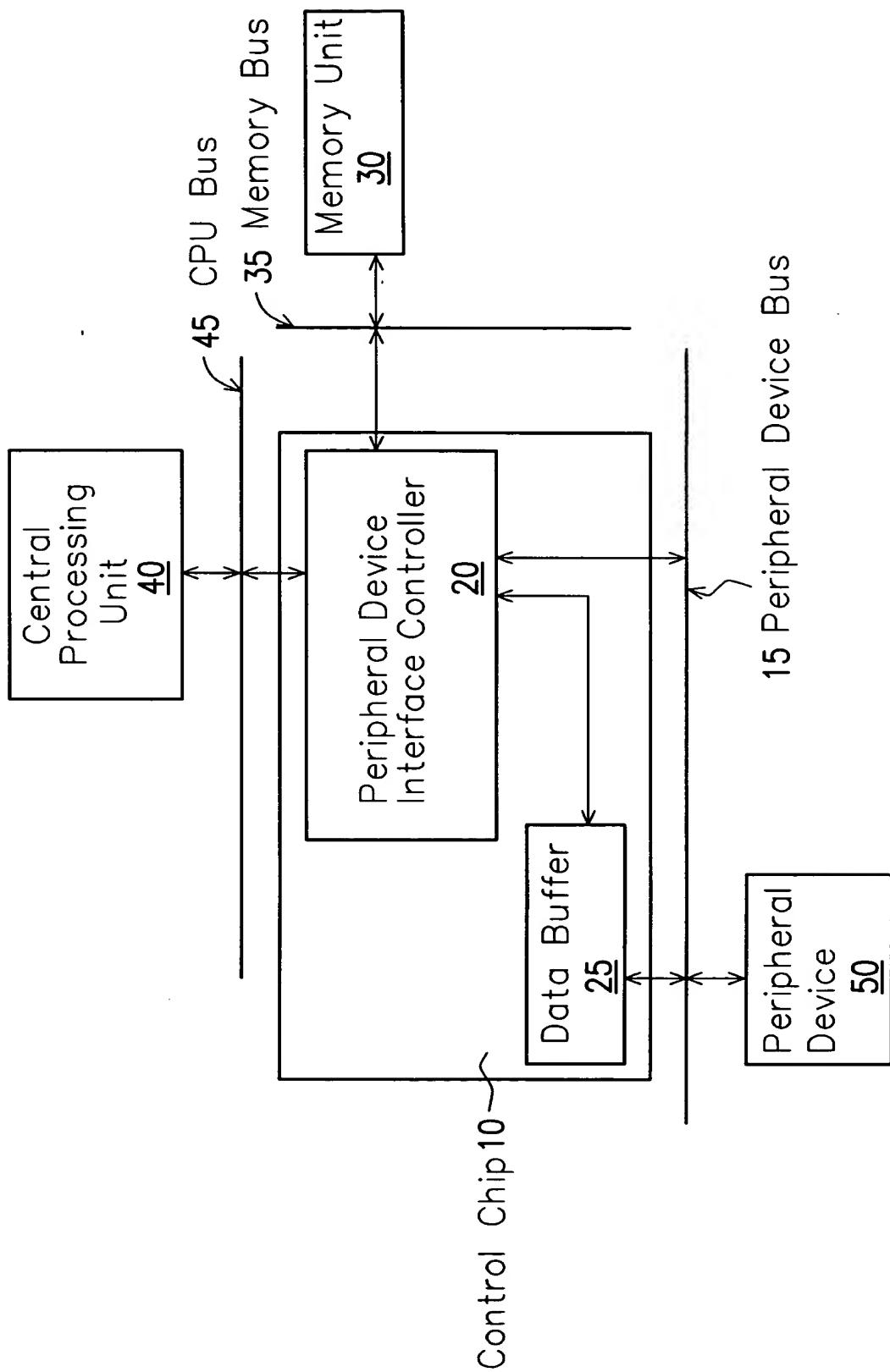


FIG. 2

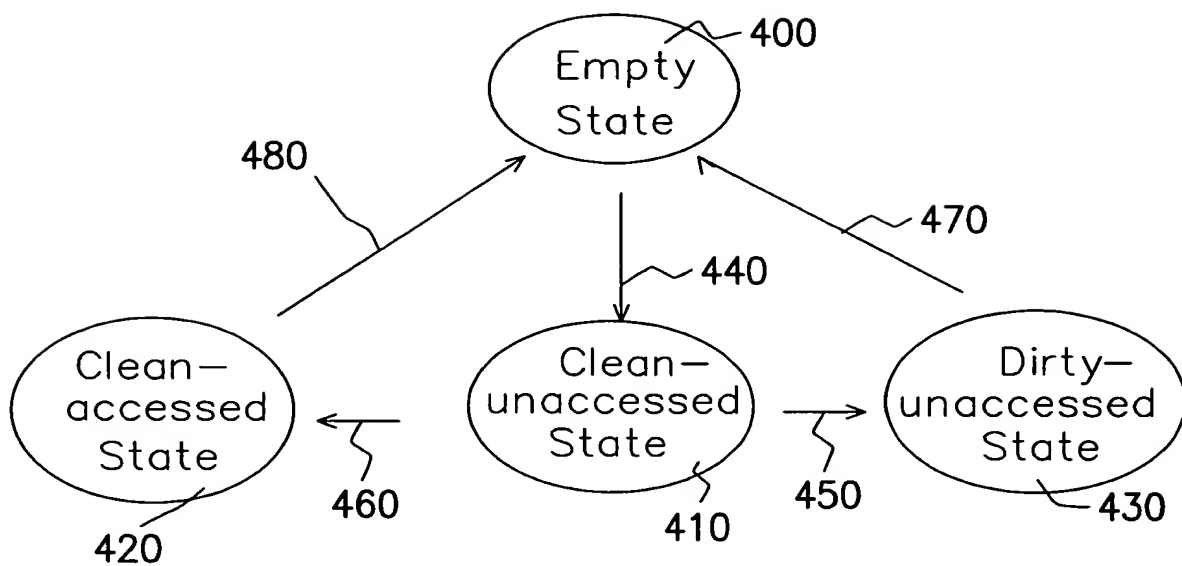


FIG. 4

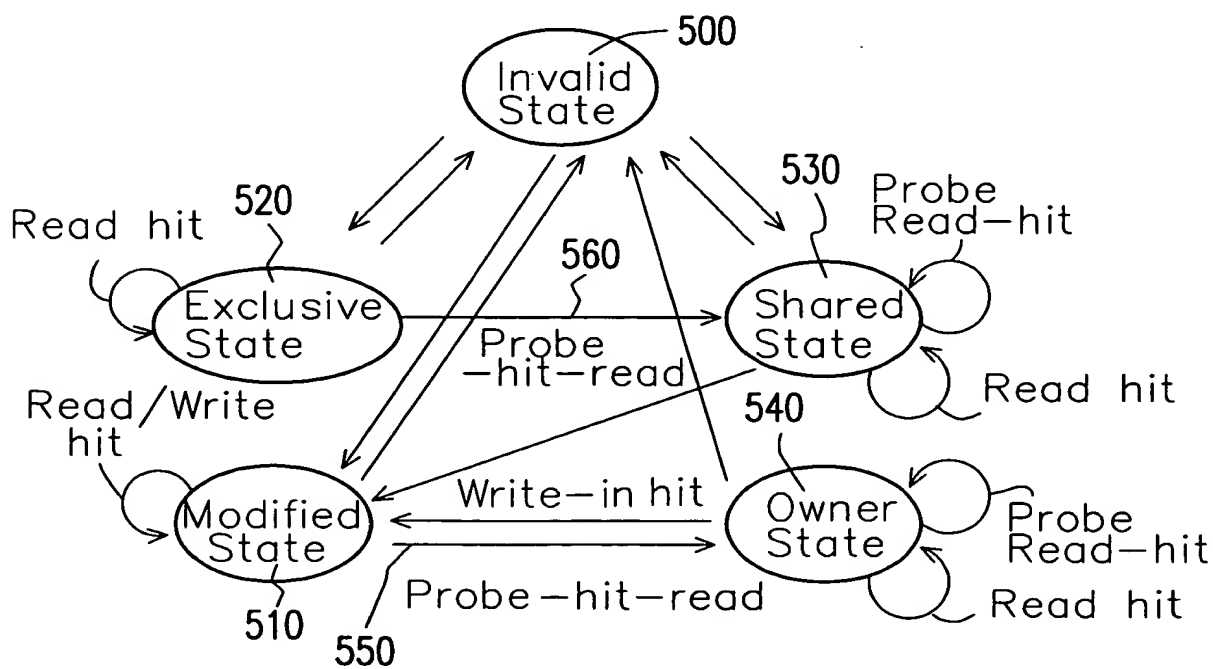


FIG. 5